Electronic Version
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Claims

[c1] 1.A system for implementing arbitration between one or more shared peripheral core devices in a system on chip (SOC) integrated circuit architecture, comprising:
a first microprocessor in communication with a first system bus;
a second microprocessor in communication with a second system bus;
at least one peripheral core device accessible by both said first microprocessor and said second microprocessor; and
an arbitration unit in communication with said first system bus and said second system bus;
wherein said arbitration unit is configured to control communication between said at least one peripheral core device and said first and second microprocessors.

[c2] 2.The system of claim 1, further comprising a plurality of arbitration units, wherein each of said plurality of arbitration units is configured to control communication between said first system bus and said second system bus, and a group of peripheral core devices associated therewith.

[c3] 3.The system of claim 1, wherein said arbitration unit further comprises:
a first buffer device coupled to said first system bus;
a second buffer device coupled to said second system bus;
input multiplexing circuitry in communication with said first buffer device, said second buffer device and said at least one peripheral core device; and
arbitration logic in communication with said first buffer device, said second buffer device and said input multiplexing circuitry.

[c4] 4.The system of claim 3, wherein:
said arbitration logic is configured to detect a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors;
said arbitration logic is further configured to determine the existence of a free peripheral from said at least one peripheral core device; and
said arbitration logic is further configured to implement communication between a determined free peripheral and said requesting one of said first and second microprocessors;
wherein said arbitration logic is further configured to inform said requesting one of said first and second microprocessors whenever no free peripheral is presently

available.

[c5] 5.The system of claim 4, wherein said arbitration unit is configured to internally note an assignment between a free peripheral and a requesting one of said first and second microprocessors.

[c6] 6.The system of claim 4, wherein:
said at least one peripheral core device is configured to communicate data externally from the (SOC) integrated circuit architecture through an external output path; and
said arbitration unit further comprising external multiplexing circuitry in communication with said at least one peripheral core device and said external output path.

[c7] 7.The system of claim 4, wherein:
said at least one peripheral core device is configured to communicate data to and from the (SOC) integrated circuit architecture through an external bus; and
said arbitration unit further comprising external multiplexing circuitry in communication with said at least one peripheral core device and said external output path.

[c8] 8.The system of claim 7, wherein:
said arbitration unit is configured to internally note an assignment between a free peripheral and a requesting one of said first and second microprocessors; and

said arbitration unit is configured to maintain said assignment until a response is received from said free peripheral indicating a completed data transfer.

[c9] 9.The system of claim 4, wherein:
said at least one peripheral core device is configured to communicate data to and from the (SOC) integrated circuit architecture through an associated external connection for each of said first and second microprocessors; and
said arbitration unit further comprising external multiplexing circuitry in communication with said at least one peripheral core device and said external connections; and
said arbitration unit further comprising an external buffer device coupled between said external multiplexing circuitry and said external connections.

[c10] 10.The system of claim 9, wherein:
said arbitration unit is configured to receive incoming data from one of said external connections and identify a target destination for said incoming data;
said arbitration unit is configured to internally note an assignment between a free peripheral and said target destination; and
said arbitration unit is configured to maintain said assignment until the completion of a completed data

transfer between said one of said external connections and said target destination, through said free peripheral.

[c11] 11.A method for implementing arbitration between one or more shared peripheral core devices in a system on chip (SOC) integrated circuit architecture, the method comprising:
configuring a first microprocessor in communication with a first system bus;
configuring a second microprocessor in communication with a second system bus;
configuring at least one peripheral core device to be accessible by both said first microprocessor and said second microprocessor; and
configuring an arbitration unit in communication with said first system bus and said second system bus, wherein said arbitration unit controls communication between said at least one peripheral core device and said first and second microprocessors.

[c12] 12.The method of claim 11, further comprising a configuring plurality of arbitration units to control communication between said first system bus and said second system bus, and a group of peripheral core devices associated therewith.

[c13] 13.The method of claim 11, wherein said arbitration unit

further comprises:

a first buffer device coupled to said first system bus;

a second buffer device coupled to said second system bus;

input multiplexing circuitry in communication with said first buffer device, said second buffer device and said at least one peripheral core device; and

arbitration logic in communication with said first buffer device, said second buffer device and said input multiplexing circuitry.

[c14] 14.The method of claim 13, wherein:

said arbitration logic detects a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors;

said arbitration logic determines the existence of a free peripheral from said at least one peripheral core device; and

said arbitration logic implements communication between a determined free peripheral and said requesting one of said first and second microprocessors, and informs said requesting one of said first and second microprocessors whenever no free peripheral is presently available.

[c15] 15.The method of claim 14, wherein said arbitration unit internally notes an assignment between a free peripheral

and a requesting one of said first and second microprocessors.

[c16] 16.The method of claim 14, wherein:
said at least one peripheral core device communicates data externally from the (SOC) integrated circuit architecture through an external output path; and
said arbitration unit further includes external multiplexing circuitry in communication with said at least one peripheral core device and said external output path.

[c17] 17.The method of claim 14, wherein:
said at least one peripheral core device communicates data to and from the (SOC) integrated circuit architecture through an external bus; and
said arbitration unit further includes external multiplexing circuitry in communication with said at least one peripheral core device and said external output path.

[c18] 18.The method of claim 17, wherein:
said arbitration unit internally notes an assignment between a free peripheral and a requesting one of said first and second microprocessors; and
said arbitration unit maintains said assignment until a response is received from said free peripheral indicating a completed data transfer.

[c19] 19.The method of claim 14, wherein:
said at least one peripheral core device communicates data to and from the (SOC) integrated circuit architecture through an associated external connection for each of said first and second microprocessors; and
said arbitration unit further includes external multiplexing circuitry in communication with said at least one peripheral core device and said external connections; and
said arbitration unit further includes an external buffer device coupled between said external multiplexing circuitry and said external connections.

[c20] 20.The method of claim 19, wherein:
said arbitration unit receives incoming data from one of said external connections and identifies a target destination for said incoming data;
said arbitration unit internally notes an assignment between a free peripheral and said target destination; and
said arbitration unit maintains said assignment until the completion of a completed data transfer between said one of said external connections and said target destination, through said free peripheral.